8051 INTERFACING TO EXTERNAL MEMORY

Semiconductor memory

- Primary memory
- Storage for code & data

SEMICONDUCTOR MEMORY

Memory capacity

- **The number of bits that a semiconductor memory chip can store is called chip capacity.**
- **It can be in units of Kbits (kilobits), Mbits (megabits), and so on.** (eg.1bit,4bit,8bit,16 bit)
- 1 byte= 8bit,1 nibble=4 bit

Memory Organization

- Memory chip contains 2^x locations,x=no.of address pins
- Each pin contain y bis,y=no.of data pins on chip
- Entire chip contains 2^x X y bits.

SEMICONDUCTOR MEMORY

Speed

- The speed of the memory chip is commonly referred to as its *access time.*
- The access time of memory chips varies from a few nanoseconds to hundreds of nanoseconds, depending technology used in the design & fabrication process.

x	2^x
10	1K
11	2K
12	4K
13	8K
14	16K
15	32K
16	64K
17	128K
18	256K
19	512K
20	1M
21	2M
22	4M
23	8M
24	16M
25	32M
26	64M
27	128M

Table 14–1 Powers of 2

ROM(read-only memory)

- **It does not lose its contents when the power is turned off.**
- **ROM (*nonvolatile* memory).**

5 types of ROM

1. PROM(Programmable ROM)/OTP(1time Programmable):-burning ROM,burns info
2. EPROM(Erasable Programmable ROM)/UV-Eprom :-program memory chip, erase 1000 times, erasing time=20 mins.
3. EEPROM(E^2PROM)-(electrically erasable programmable ROM)-cost more, electrical erase
4. Flash Memory EPROM:-1 can erase desired section/byte
5. Mask ROM:-content programmed by IC manufacturer not by user

RAM (random access memory)(volatile)(RAWM)

- loss of data after power cutting off

3 types:-

1. SRAM (static RAM):-Storage cells in SRAM are made of flip-flops ,high capacity
2. NV-RAM(NV-RAM (nonvolatile RAM):-it allows the CPU to read and write to it, but when the power is turned off the contents are not lost.
3. DRAM (dynamic RAM):-uses a capacitor to store each bit requires constant refreshing due to leakage

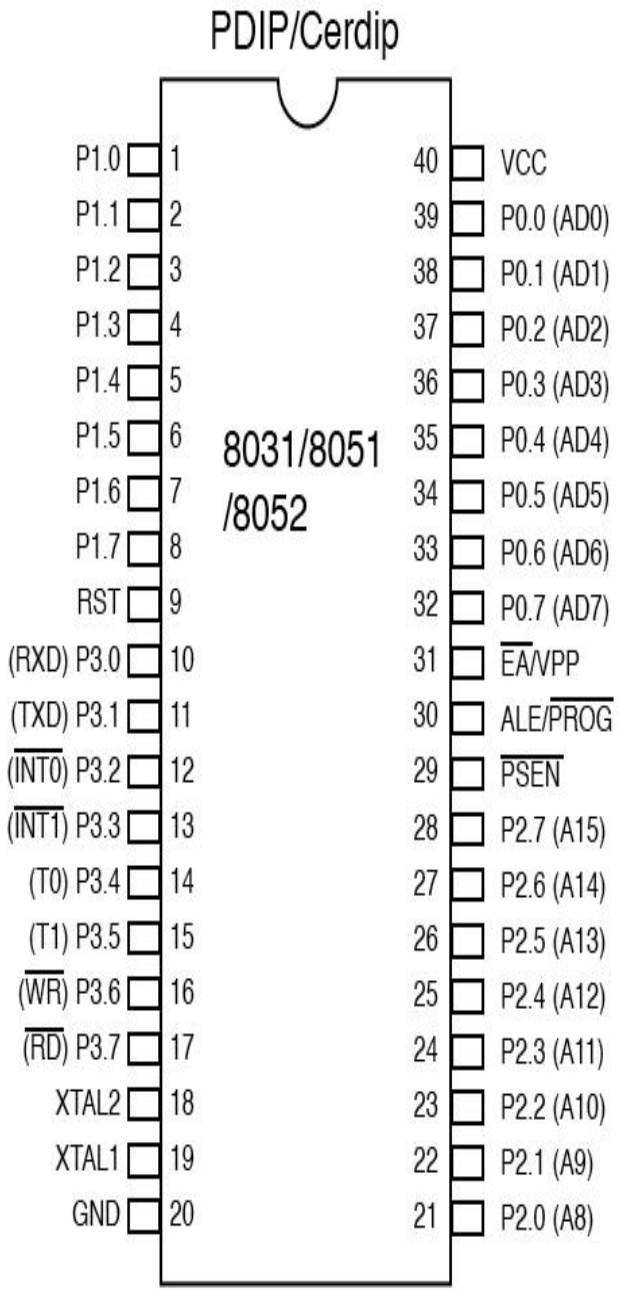
8051 Pin Diagram

EA pin

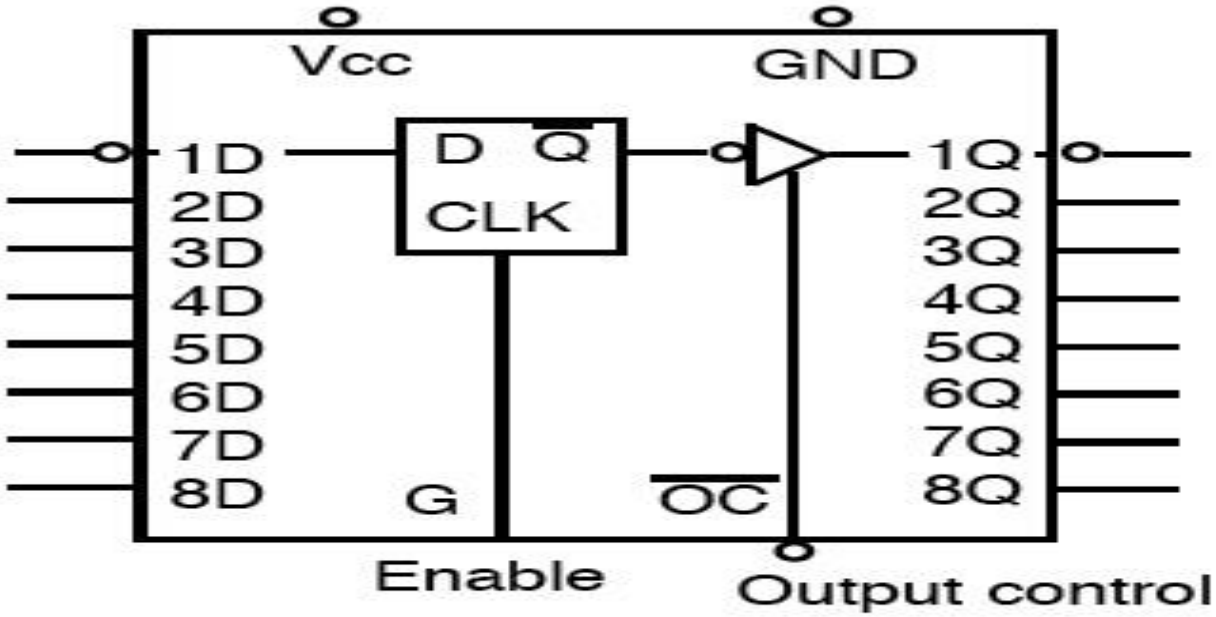
- EA = Vcc to indicate that the program code is stored in the μC's on-chip ROM.
- EA = GND to indicate that the program code is stored in external ROM

When ALE=0,P0=use as data

When ALE=1,P0=use as address



74LS373 D Latch

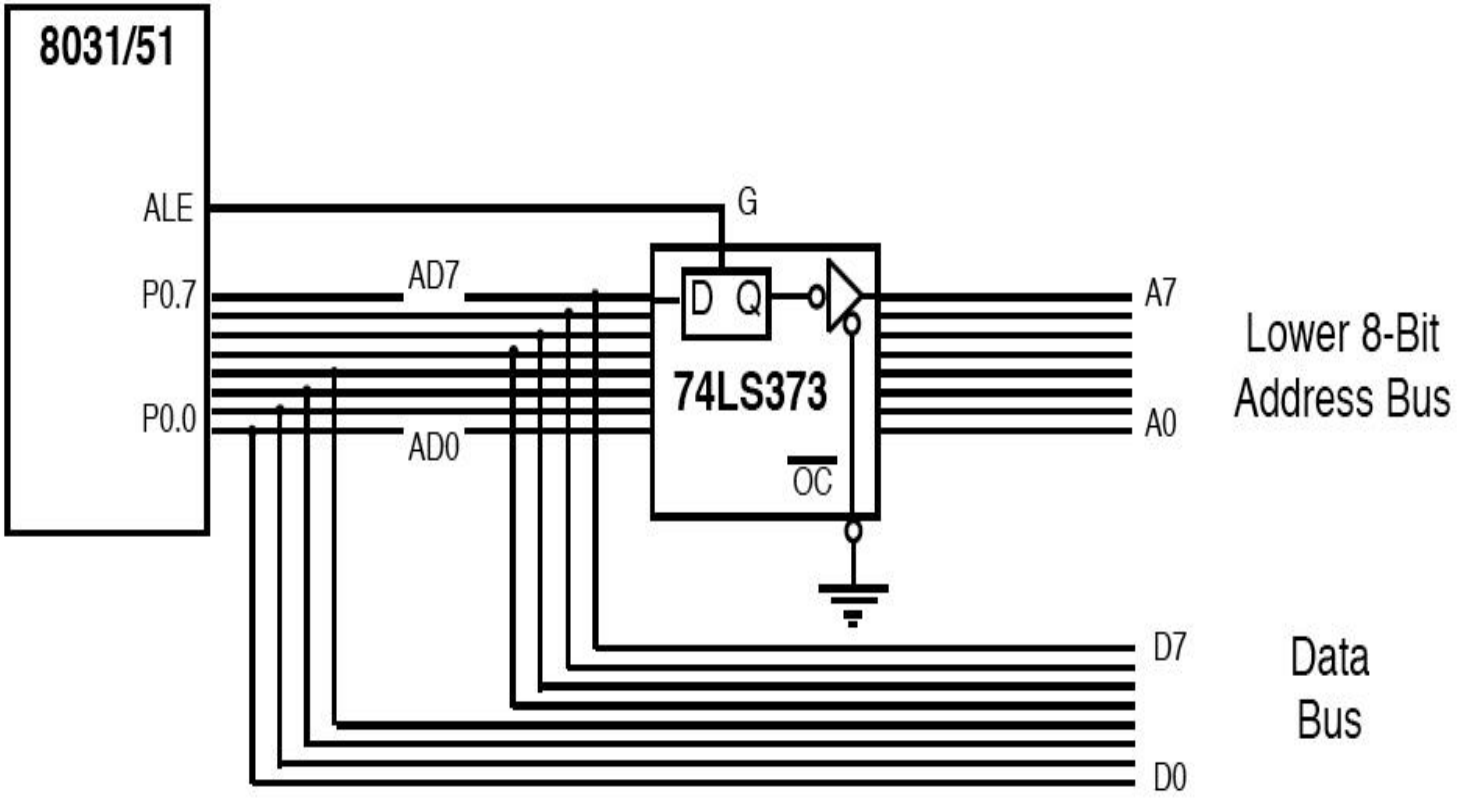


Funtion Table

Output control	Enable G	Enable D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

Address/Data Multiplexing

- P0 and P2 role in providing addresses



Data, Address, and Control Buses for the 8031

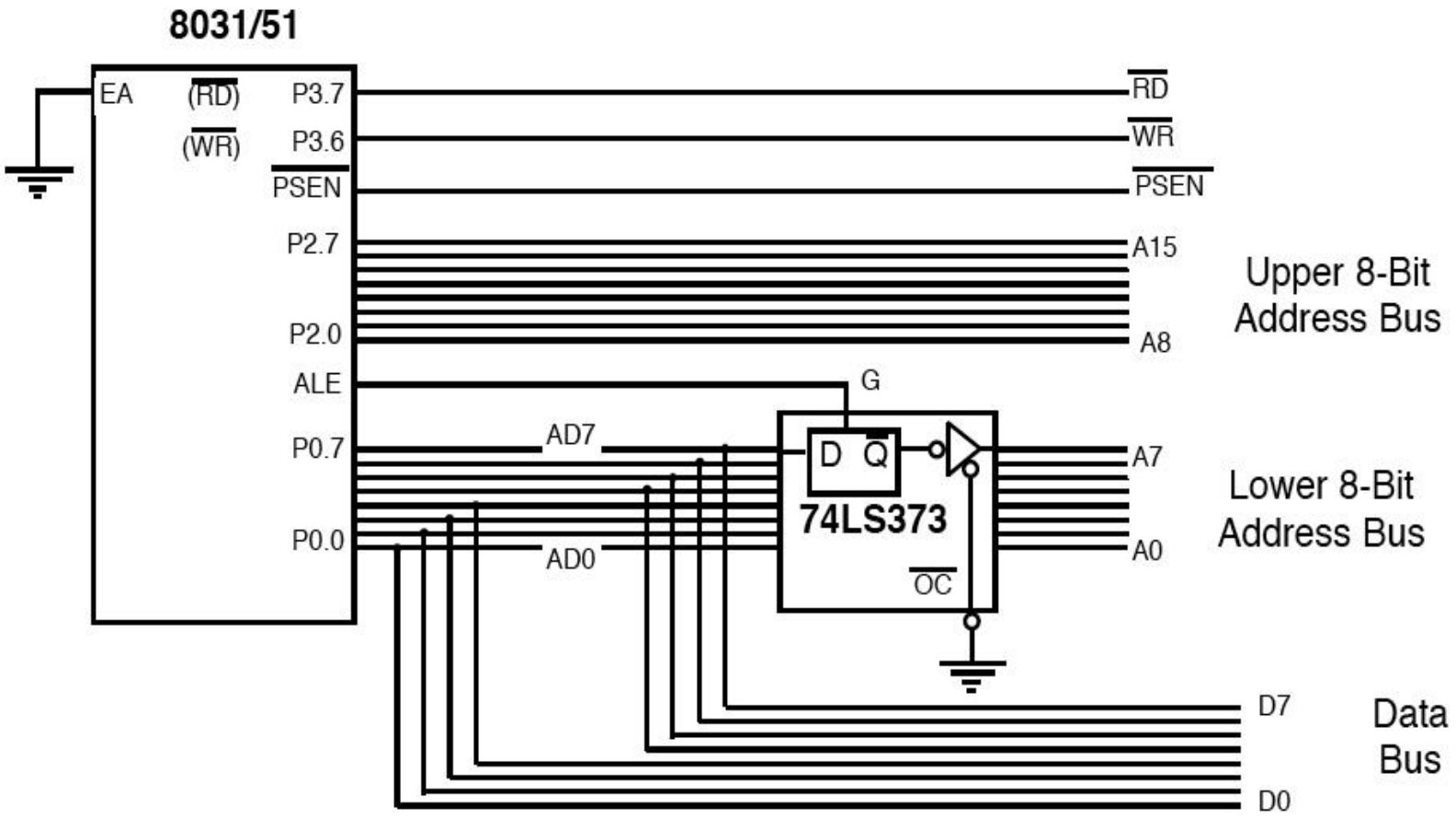
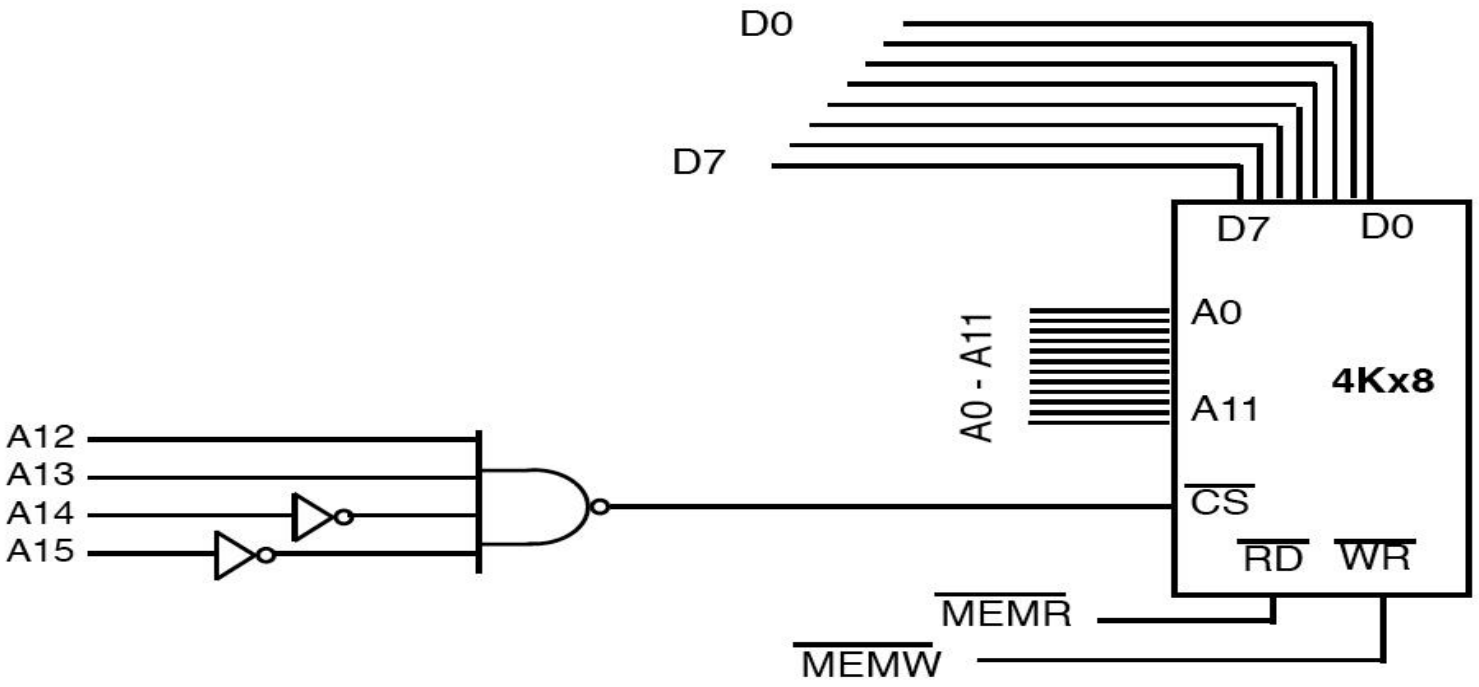


Figure 14–10

Logic Gate as Decoder

- **Simple logic gate address decoder**

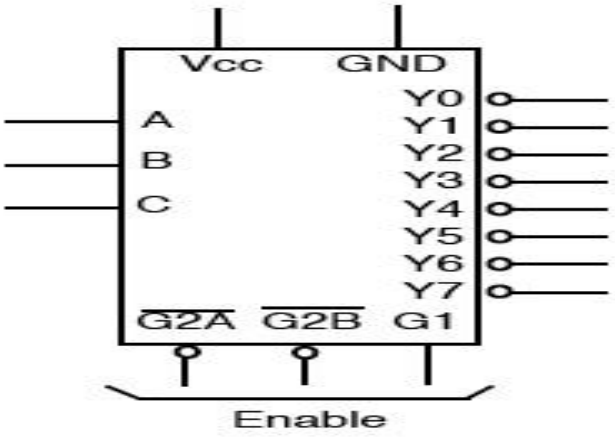


Simple logic gate address decoder

- Using a combination of NAND gates and inverters, one can decode any address range.
- A15 – A12 = 0011 in order to select the chip. This results in the assignment of addresses 3000H to 3FFFH to this memory chip.

Using the 74LS138 3-8 decoder

Block Diagram



Function Table

Inputs					Outputs							
Enable		Select										
G1	G2	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Looking at the design in Figure 14-6, find the address range for the following.
(a) Y4, (b) Y2, and (c) Y7.

Solution:

(a) The address range for Y4 is calculated as follows.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1

The above shows that the range for Y4 is 4000H to 4FFFH. In Figure 14-6, notice that A15 must be 0 for the decoder to be activated. Y4 will be selected when A14 A13 A12 = 100 (4 in binary). The remaining A11 - A0 will be 0 for the lowest address and 1 for the highest address.

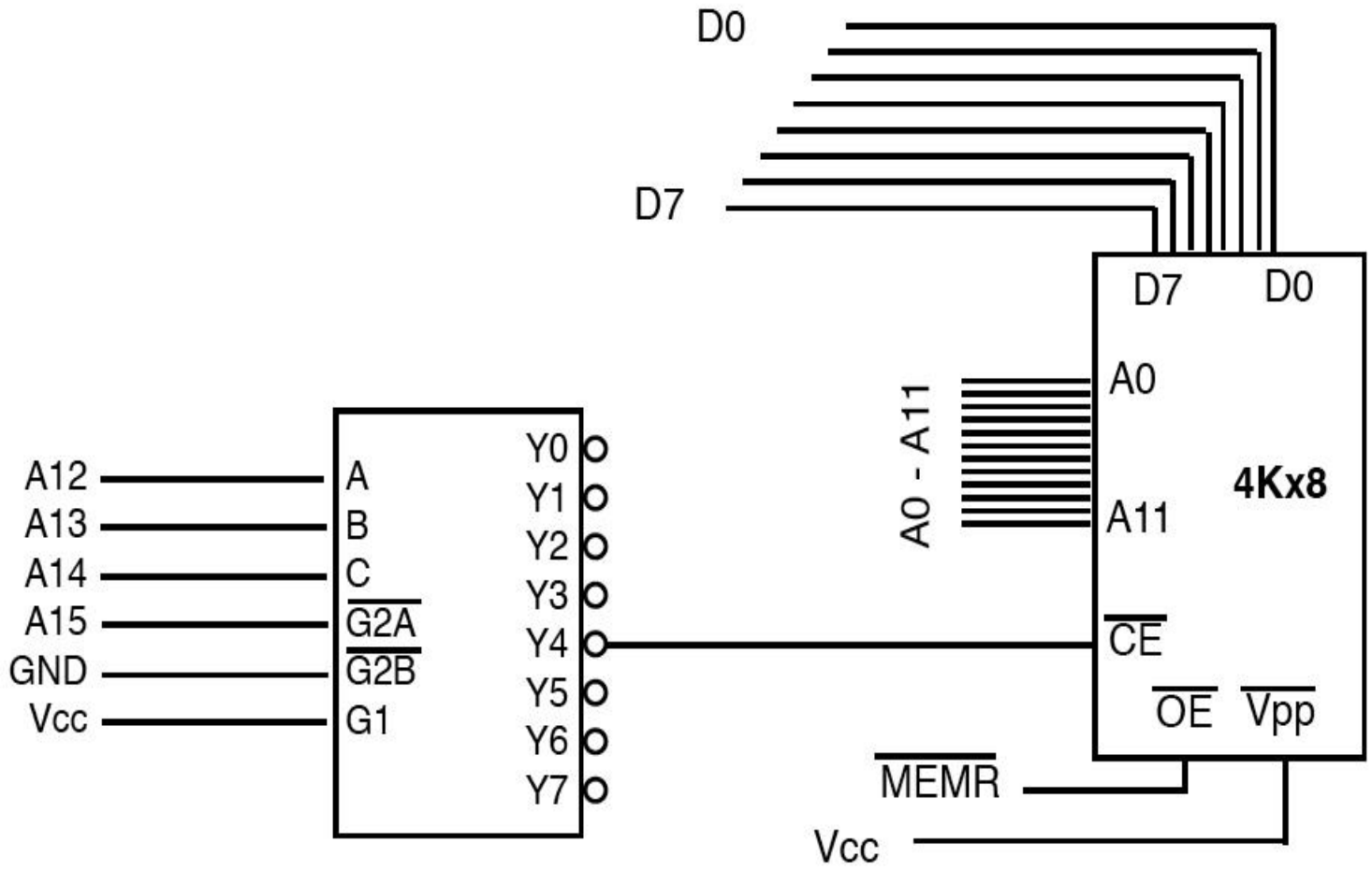
(b) The address range for Y2 is 2000H to 2FFFH.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1

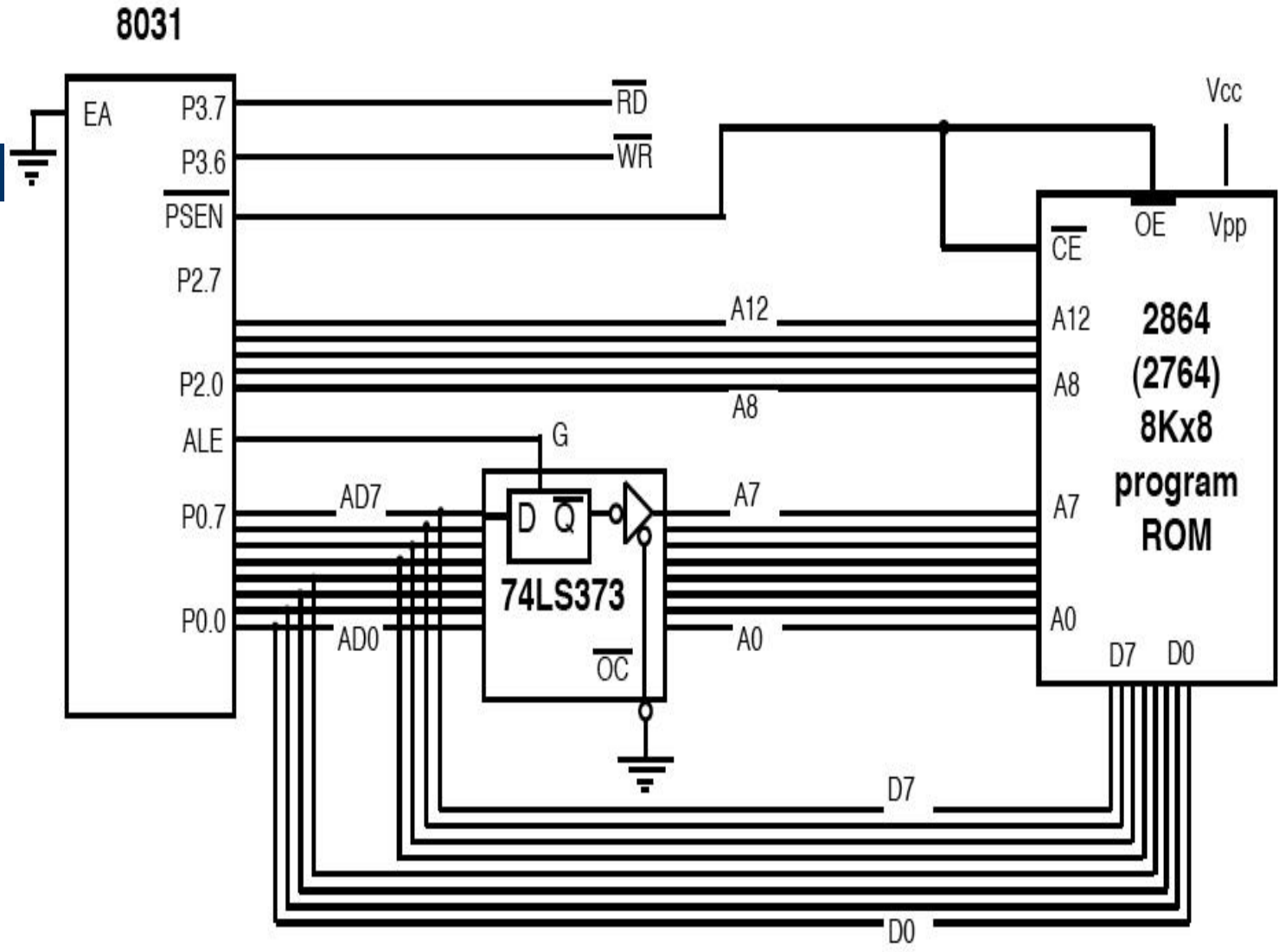
(c) The address range for Y7 is 7000H to 7FFFH.

A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

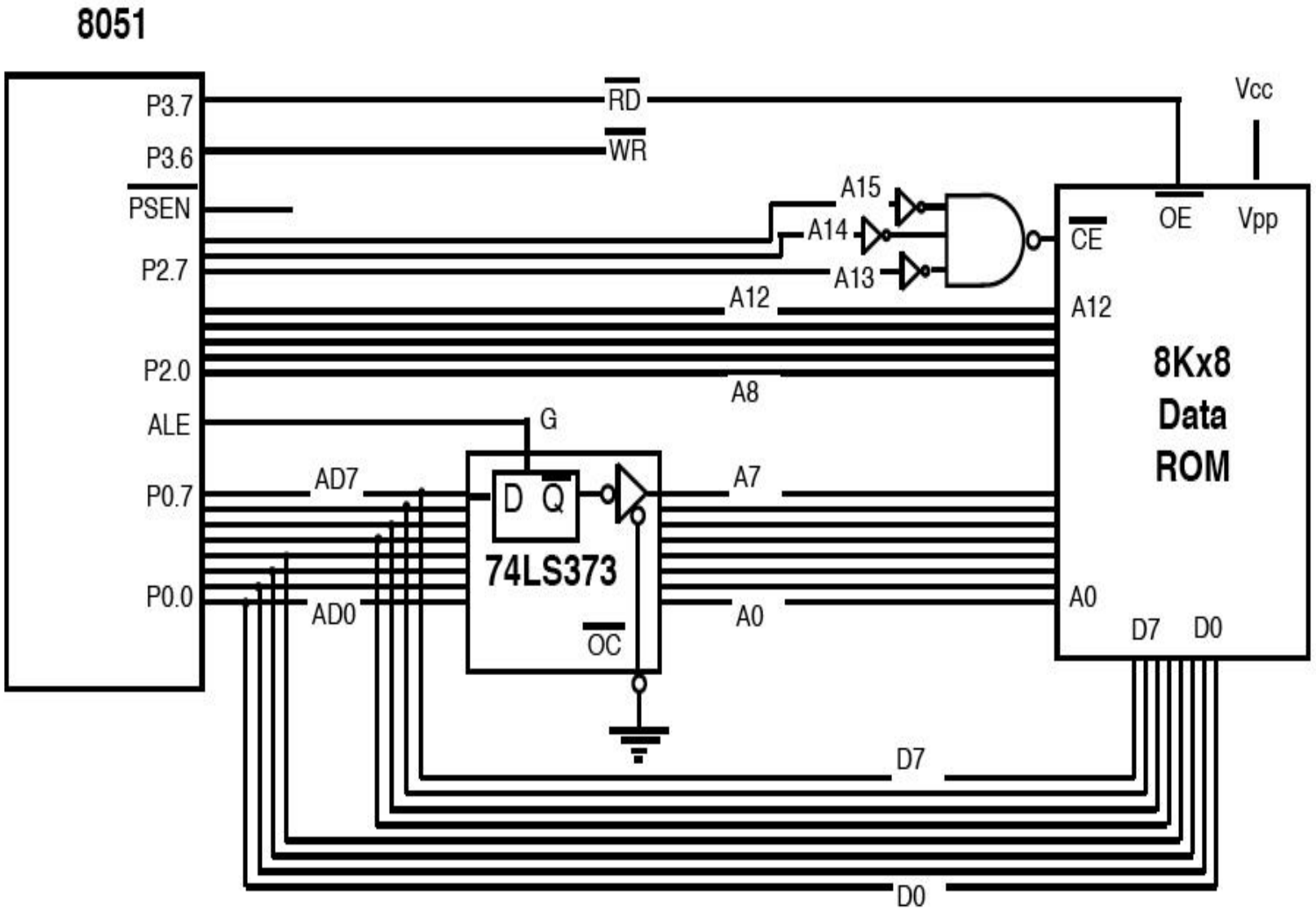
74LS138 as Decoder



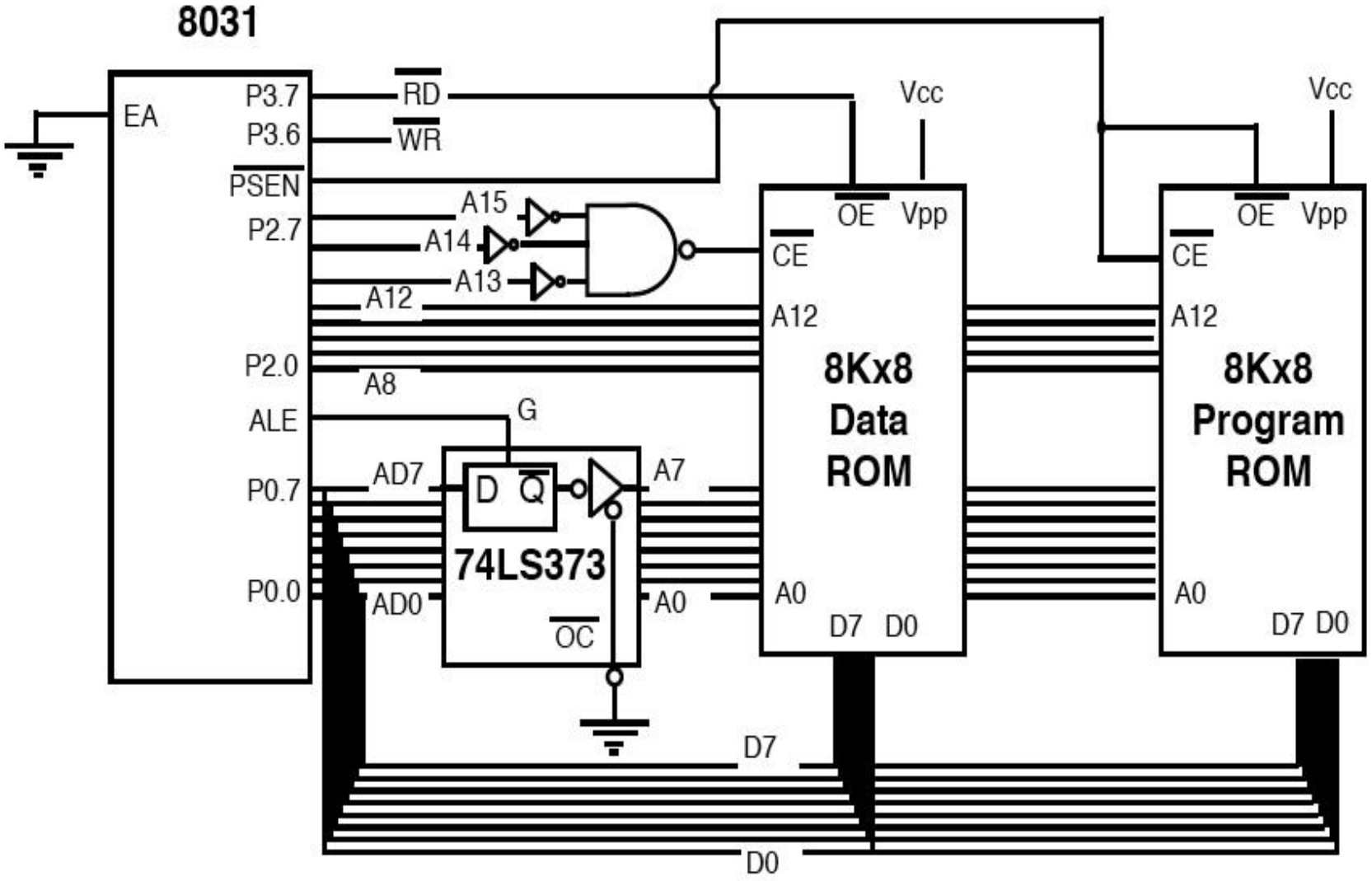
8031/51 INTERFACING WITH EXTERNAL PROGRAM ROM



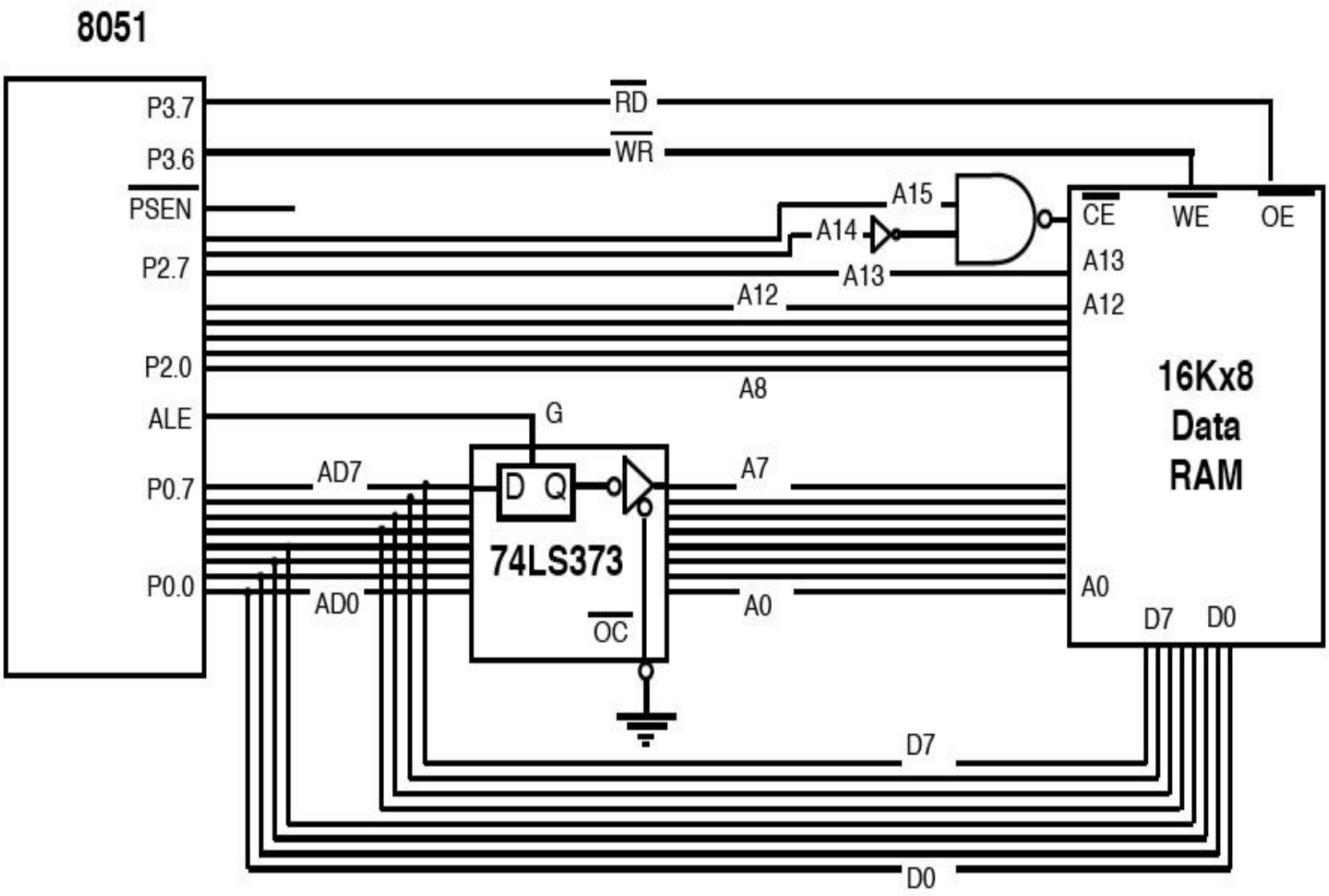
8051 Connection to External Data ROM



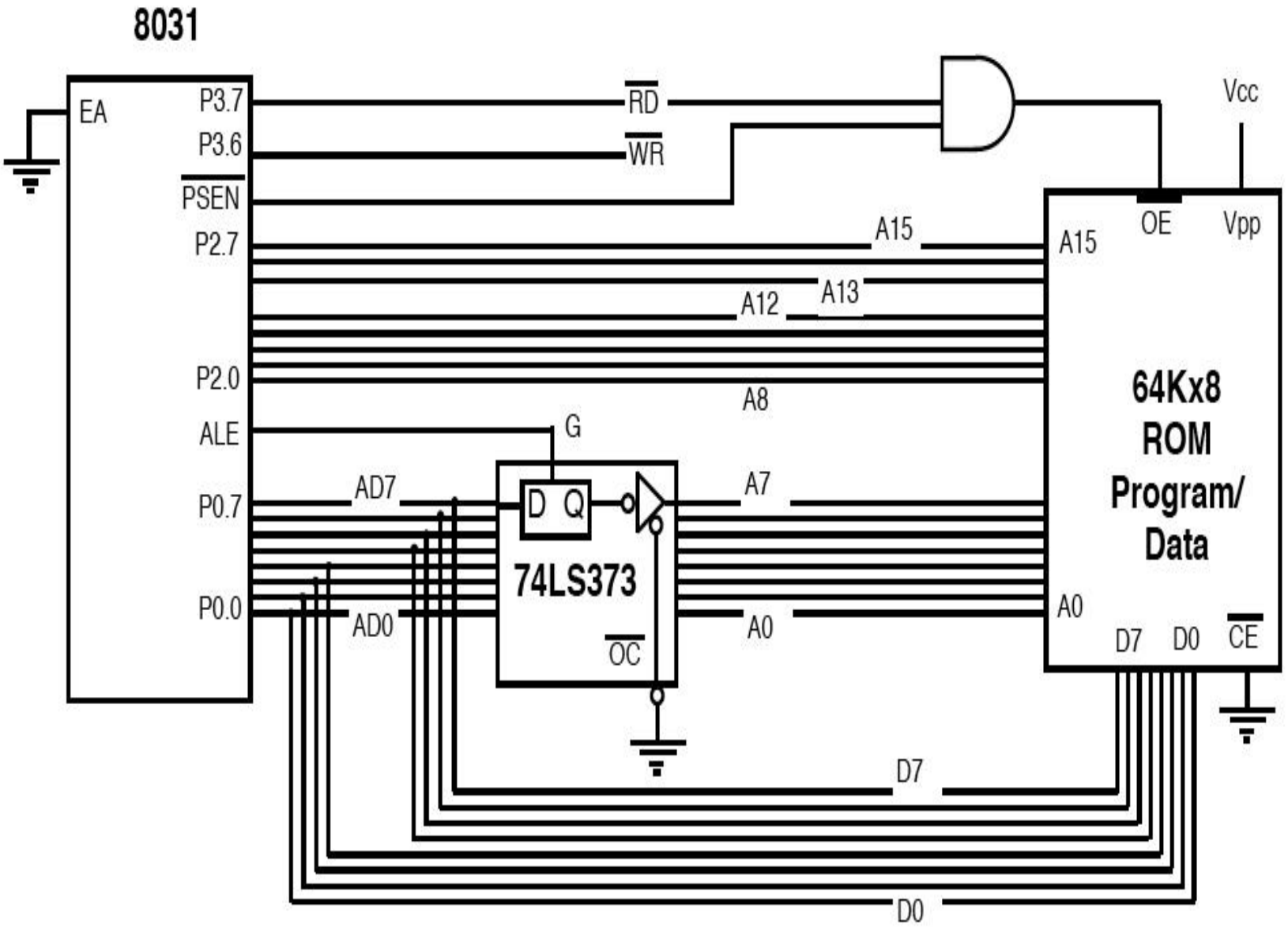
8031 Connection to External Data ROM and External Program ROM



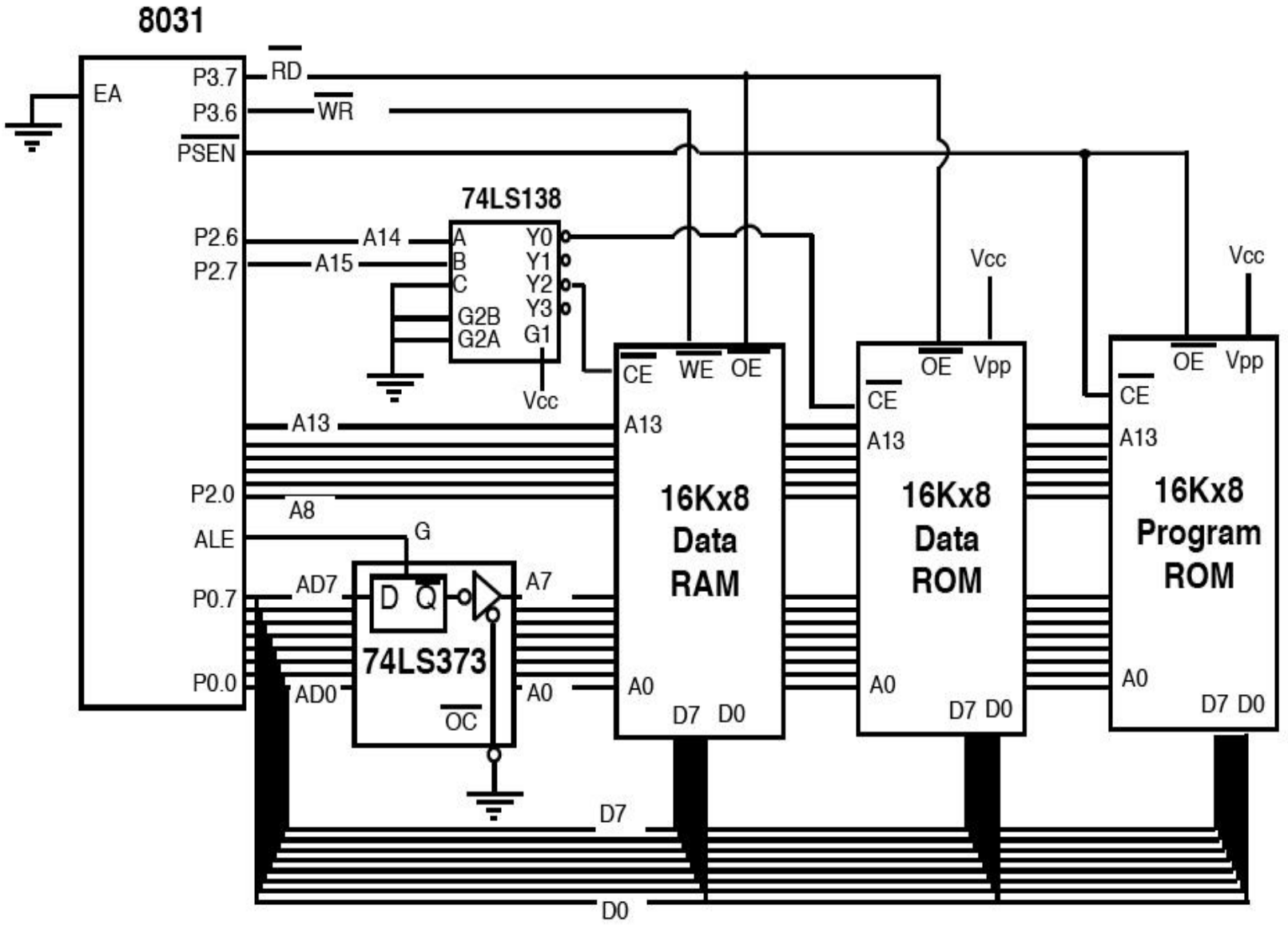
8051 Connection to External Data RAM



A Single ROM for Both Program and Data



8031 Connection to External Program ROM, Data RAM, and Data ROM



Interfacing to large external memory